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FLIP-FLOP CIRCUIT

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FLIP-FLOP CIRCUIT

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Claims

1. A flip-flop circuit of CMOS construction characterized in that the respective outputs of the data storage circuit (6) on the master side made up of a plurality of logic gates are connected to one electrode through the medium of switching circuits (7, 8) that are made up of at least 2 series MOS transistors that transfer input data, the respective outputs of the data storage circuit (9) on the slave side made up of a plurality of logic gates are connected to the other electrode through the medium of switching circuits (10, 11) made up of at least two series MOS transistors that transfer the data from the master side to the slave side, and the respective outputs of the data storage circuit (6) of the master side are connected directly, or are connected through the medium of the logic gate (12), to the gate of one or more of the MOS transistors of the respective series connected MOS transistors of the switching circuits (10, 11) of the slave side.

2. A flip-flop circuit characterized in that, in the flip-flop circuit recorded in Paragraph 1 of the patent claims, the data transfer clock for the master side and the data transfer clock for the slave side use the same signal.

Detailed explanation of the invention

Industrial application field

This invention relates to an IC made up of a plurality of flip-flop circuits having a data transfer function, an IC made up of a plurality of flip-flop circuits having a data latching function, and an IC made up of a plurality of flip-flop circuits having a count function, such as ICs used for LCD drives and ICs used for VFD drives.

Prior art

In regard to flip-flop circuits of a CMOS construction, in the past, there was the device that used the clocked gate (1) such as is shown in Figure 1, and the device that used the transmission gate, such as is shown in Figure 2.

Here, the signal (DIN) is the input data for the flip-flop circuit, the signal (M) is the storage data for the master side, the signal M is its inverted signal, the signal (Q) is the storage data for the slave side, and signal (Q overline) is its inverted signal. Also, signal (CL) is the transmission clock, and the signal (CL overline) is its inverted signal.

The element construction for the clocked gate (1) in Figure 1 is like that of Figure 3(b). In Figure 1 and Figure 2, when the signal (CL) is "H" and the signal (CL overline) is "L," the input data at signal (DIN) is written into the storage circuit of the master side, and when the signal (CL) is "L" and the signal (CL overline) becomes "H," the data that is stored in the master side is transferred to the memory circuit of the slave side.

As it says above, with such a flip-flop circuit using a clocked gate or such a flip-flop circuit using a transmission gate, there was the problem that the gate would not operate unless the 2 signals (CL) and (CL overline) were used as the data transfer clock. Also, as is shown in Figure 5, the signal (CL) and the signal (CL overline) were opposite phase signals, and unless phase differences (t_1, t_2) were made as small as possible, there was the problem that the flip-flop circuit operated erroneously. As is shown an Figure 6, in particular, if the number of flip-flop circuits which compose a shift register was made n, the converter buffers (3, 5) which generate the shift register transfer clock signals (CL) and signals (CL overline) would come to drive the gates of 4 x n units of MOS transistors, and MOS transistors with large capacitances became necessary (For example, if n is assumed to be 100, the number of MOS transistors which the inverter buffers (3, 5) drive becomes 400.)

Furthermore, if the capacitances of the inverter (4) that inverted the phase of the signal (CL) were not made large compared to the size of the inverter buffer (5), there was the problem that the phase difference (t_1, t_2) could not be made small. Also, by making the capacitance of the MOS transistor large in this manner a large surface area was required, and there were problems the surface area of the IC becoming large and the unit cost of the IC becoming high. In addition, because the capacitances of the MOS transistors were large, the punch-through current for each inverter (3, 4, 5) became large; and as the number of gates for the MOS transistors which the inverter buffer (4, 5) drove increased, the driving power supply became large, the charging current for the inverter buffer (4, 5) became large,

and there was the problem that the consumed current of the IC became large.

Purpose

This invention solve these types of problem points, and its purpose is to offer a flip-flop circuit of a CMOS construction which operates with 1 transfer clock.

Abstract

The flip-flop circuit of a CMOS construction of this invention is characterized in that the input data is written to a master side data storage circuit by a switching circuit made up of a MOS transistor of one channel, the storage data of the master side is transferred to the slave side data storage circuit by a switching circuit made up of a MOS transistor of the other channel, and the transfer clock for the master side and the transfer clock for the slave side use the same signal.

Application Examples

Below, a detailed explanation is given in regard to this invention based on application examples.

Figure 7 is an example of a basic circuit of a flip-flop circuit of this invention. As for the signal (M) of the master side data storage circuit (6), when the input data signal (DIN overline) (the opposite phase signal for the input data signal (DIN)) is "H" (V_{DD} level) and the transfer clock signal (CL1) is " H," the switching circuit (8) made up of an NMOS transistor is turned ON and forcibly becomes "L" (V_{SS} level), and in the same manner, the switching circuit (7) made up of an NMOS transistor

is turned OFF and the signal (M overline) becomes "H." In the event the input data signal (DIN) is "H," the switching circuit (7) is turned ON, the signal (M overline) is forcibly made "L," the switching circuit (8) is turned OFF, and the signal (M) becomes "H." In this way, the input data (DIN) can be transferred to the master side data storage circuit (6) when the transfer clock signal (CL1) is "H." In the transferring of the storage data of the master side to the data storage circuit of the slave side, if the signal (CL2) is made "L," when the master side signal (M) is "H" and the signal (M overline) is "L," the switching circuit (11) made up of a PMOS transistor on the slave side is turned ON, and the signal (Q) is forcibly made "H"; in the same manner, when the switching circuit (10) made up of a PMOS transistor is turned OFF, the signal (Q overline) becomes "L." Also, when the master side signal (M) is "L" and the signal (M overline) is "H," the switching circuit (10) is turned ON, and the switching circuit (11) is turned OFF, the signal (Q overline) is forcibly made "H" and the signal (Q) becomes "L."

In this way the storage data of the master side is transferred to the slave side data storage circuit (9) when the transfer clock signal (CL2) is "L."

As was presented above, in the circuit of Figure 7, when the signal (CL1) is "H" the input data can be transferred to the data storage circuit of the master side, and when the signal (CL2) is "L" the storage data of the master side can be transferred to the storage circuit of the slave side. Since the signal (CL1) and the signal (CL2) operate respectively at "H" and "L," the same signal can be used.

In the case of Figure 7, the capacitances of the switching circuits (7, 8) used for data transfer of the master side must be

larger than the capacitance of the logic gate of the data storage circuit (6), but by means of reducing the resistor (18) [sic; should be 13] of Figure 8, the capacitances of the switching circuits (7, 8) can be made small compared to that of Figure 7.

Furthermore, the inverter buffer (12) of Figure 8 is used as a data buffer for the master side, and by making the capacitance larger, at the time of taking the data of the master side to an external section, it is more effectively used than taking the signal (M) and the signal (M overline) out directly. [TN: Not sure of this paragraph.]

Figure 9 is an example according to this invention of a flip-flop circuit used for 1/2 cycle. The signal (Q overline) is connected to the signal (DIN) in Figure 7, and the signal (Q) [is connected] to the signal (DIN overline). In the flip-flop circuit using the clocked gate of the example from the prior art, it was made a flip-flop circuit for 1/2 cycle by connecting the signal (Q overline) to the signal (DIN) as in Figure 4.

Figure 10 is an example of this invention of a flip-flop circuit having a reset function, and it is given the reset function by using one of the logic gates of the master side data storage circuit (6) and the slave side data storage circuit (9) as the 2 input NAND gates (14). The reset signal (RES overline) is normally "H," when it is "L," the signal (M overline) and the signal (Q overline) are made "H," the signal (M) and the signal (Q) become "L," and the master side data storage circuit (6) and the slave side data storage circuit (9) are reset. Also, as for the NMOS transistor (15) that is connected in series with the master side switching circuit (7), the signal (M overline) of the master side inhibits the input data signal (DIN) from becoming "L" when it is "H" when the transfer clock signal (CL1) is "H,"

but it is unnecessary only when the timing at which the signal (CL1), at which the reset signal (RES overline) becomes "L," is "L," when the input data signal (DIN) is "L," or when the input data signal (DIN) this "L" [sic].

Figure 11 is another example based on this invention of a flip-flop circuit with a reset function: by means of making the reset signal (RES overline) "L," the PMOS transistor (16) is turned ON, signal (M overline) and signal (Q overline) are forcibly made "H," the signal (M) and the signal (Q) are made "L," and the master side data storage circuit (6) and the slave side data storage circuit (9) are reset. Here, the NMOS transistor of Figure 11 has the same function as that of Figure 10.

Effects

As was presented above, according to this invention, the transfer clock for the master side and the transfer clock for the slave side flip-flop circuits can use the same signal, and it has the effect that the signals can be reduced to 1 compared with the 2-phase clock used in the past, and also, it has the effect that erroneous operations due to the phase differences (t_1, t_2) in the case of the 2-phase clock is the eliminated. It also has the effects that: the surface area of the IC can be reduced due to the fact that there is 1 less signal, the unit cost of the IC can be lowered, and the current consumption can be reduced. In addition, according to this invention, there is also the effect that the number of elements for the flip-flop circuit can be reduced compared to those used in the past. In the case [of the circuit] used until now of Figure 1, the number of elements is

20, and in the case [of the circuit] of this invention of Figure 7, the number of elements is 16.

Now, with this invention, the master side switching circuit is constructed of NMOS transistors, and the slave side switching circuit is constructed of PMOS transistors, but the master side switching circuits can also be constructed of PMOS transistors and the slave side switching circuit of NMOS transistors.

Brief explanation of the figures

Figure 1 is a prior example of a flip-flop circuit using a clocked gate.

Figure 2 is a prior example of a flip-flop circuit using a transmission gate.

Figure 3(a) is a symbol diagram for a clocked gate, and (b) is a drawing showing the element construction for the clocked gate.

Figure 4 is a prior example of a 1/2 cycle flip-flop circuit using a clocked gate.

Figure 5 is a timing chart showing the phases for the signal (CL) and the signal (CL overline) used in Figure 1 and Figure 2.

Figure 6 is a connection example when a plurality of flip-flop circuits used in the past are used as a shift register.

Figure 7 is one example of a basic circuit for a flip-flop circuit according to this invention.

Figure 8 is one example of an application of a flip-flop circuit according to this invention.

Figure 9 is one example of a 1/2 cycle flip-flop circuit according to this invention.

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Figure 10 and Figure 11 are examples of flip-flop circuits according to this invention having a reset function.

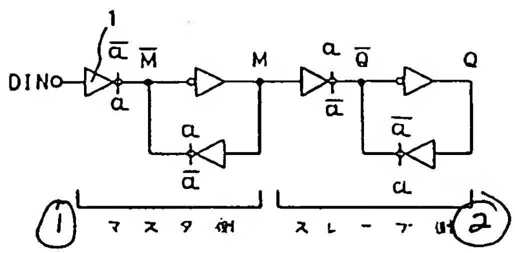

Figure 1

Key: 1 Master side
2 Slave side

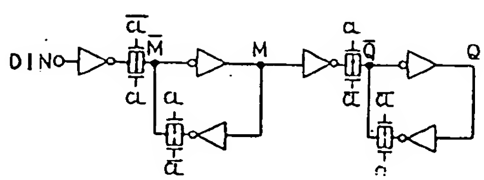

Figure 2

Key: 1 Input data
2 Flip-flop
3 N = number of units to about one hundred units

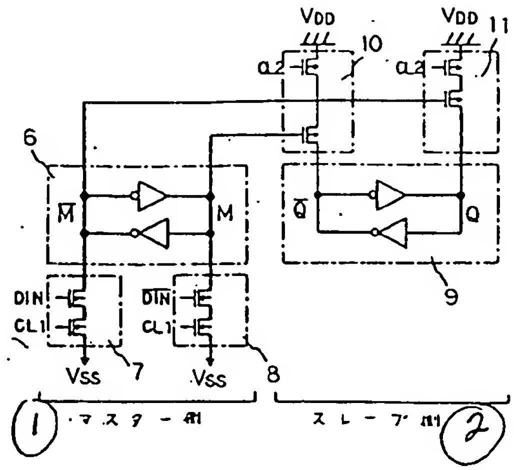

Figure 7

Key: 1 Master side
2 Slave side

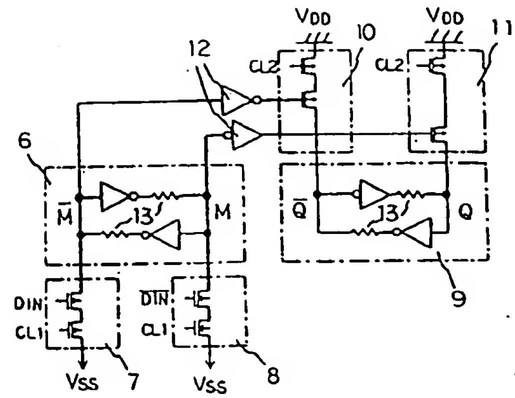

Figure 8

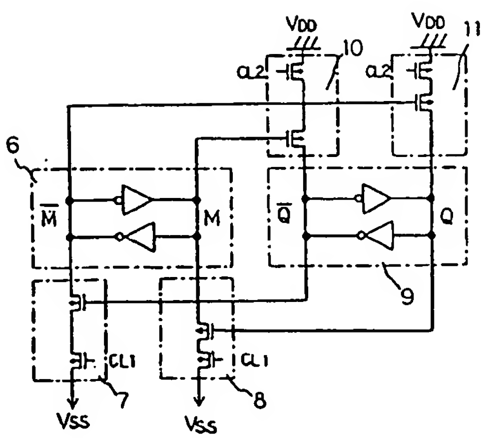

Figure 9

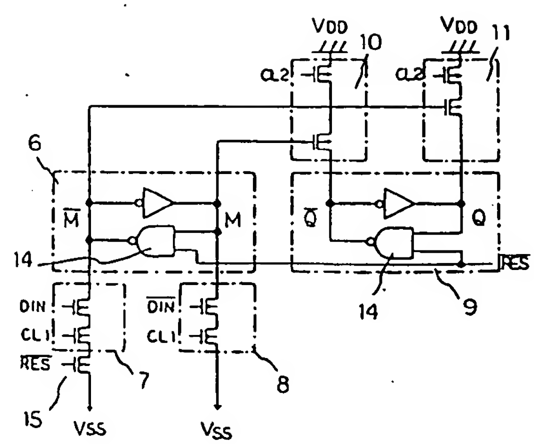

Figure 10

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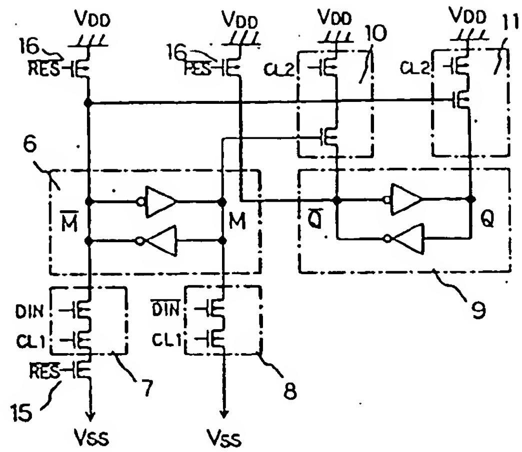

VDD
VDD
VDD
VDD
16
16
RES
RES
CL2
CL2
10
11
6
M
M
Q
Q
9
DIN
CL1
RES
DIN
CL1
7
8
15
Vss
Vss

Figure 11

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㊹発明の名称　フリップ・フロップ回路

㉑特　願　昭59-80959

㉒出　願　昭59(1984)4月20日

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明　細　書

発明の名称

フリップ・フロップ回路

特許請求の範囲

(1) 複数の論理ゲートよりなるマスタ側のデータ記憶回路6の各々の出力は、入力データを転送する少なくとも2個の直列するMOSトランジスタよりなるスイッチ回路7，8を介して一方の電極に接続され、また複数の論理ゲートよりなるスレーブ側のデータ記憶回路9の各々の出力は、マスタ側からスレーブ側へデータを転送する少なくとも2個の直列するMOSトランジスタよりなるスイッチ回路10，11を介して他方の電極に接続され、マスタ側のデータ記憶回路6の各々の出力は、スレーブ側のスイッチ回路10，11の各々の直列するMOSトランジスタの1つ以上のMOSトランジスタのゲートに直接、または論理ゲート12を介して接続されることを特徴とするCMOS構造のフリップ・フロップ回路。

(2) 特許請求の範囲第(1)項記載のフリップ・フロップ回路において、マスタ側のデータ転送クロックとスレーブ側のデータ転送クロックに同一の信号を用いることを特徴とするフリップ・フロップ回路。

発明の詳細な説明

〔技術分野〕

本発明は、LCD駆動用ICやVFD駆動用ICのような複数のフリップ・フロップ回路よりなるデータ転送機能を有するICや、複数のフリップ・フロップ回路よりなるデータ・ラッチ機能を有するICや、複数のフリップ・フロップ回路よりなるカウンタ機能を有するICに関する。

〔従来技術〕

CMOS構造のフリップ・フロップ回路に関しては、従来より第1図に示されるような、クロックド・ゲート1を用いたものや、第2図に示されるような、トランスミッション・ゲートを用いたものがあった。

ここで信号DINはフリップ・フロップ回路の入力データであり、信号Mはマスタ側の記憶データ、信号$\overline{M}$はその反転信号であり、信号Qはスレーブ側の記憶データ、信号$\overline{Q}$はその反転信号である。また信号CLは転送クロックであり、信号$\overline{CL}$はその反転信号である。

第1図中のクロックド・ゲート1の素子構成は第8図(b)のようになっている。第1図，第2図において、入力データ信号DINは信号CLが'H'，信号$\overline{CL}$が'L'のとき、マスタ側の記憶回路に書き込まれ、マスタ側に記憶されたデータは信号CLが'L'，信号$\overline{CL}$が'H'になると、スレーブ側の記憶回路に転送される。

このように、クロックド・ゲートを用いたフリップ・フロップ回路や、トランスミッション・ゲートを用いたフリップ・フロップ回路では、データ転送用のクロックとして、信号CLと信号$\overline{CL}$の2つの信号を用いなければ動作しないという問題点があった。更に信号CLと信号$\overline{CL}$は、第5図に示されるように逆相信号であり、その位相差t_1，t_2は極力小さくしなければ、フリップ・フロップ回路が誤動作するという問題点があった。特に第6図のように多数の従来のフリップ・フロップ回路よりなるシフト・レジスタの転送クロック信号CL，信号$\overline{CL}$を発生するインバータ・バッファ3，5は、シフト・レジスタを構成するフリップ・フロップ回路の数をnとすると、4×n個のMOSトランジスタのゲートを駆動することになり、能力の大きなMOSトランジスタが必要となる。(例えばnを100とすると、インバータ・バッファ3，5が駆動するMOSトランジスタの数は400となる。)

更に、信号CLの位相を反転するインバータ4の能力も、インバータ・バッファ5の大きさに比例して大きくしないと位相差t_1，t_2を小さくできないという問題があった。また、このようにMOSトランジスタの能力を大きくするということは、大きな面積を必要とする為、ICの面積が大きくなり、ICの単価が高くなってしまうという問題点もあった。その上、MOSトランジスタの能力が大きい為、各インバータ3，4，5の貫通電流が多くなり、またインバータ・バッファ4，5が駆動するMOSトランジスタのゲート数が多い為、駆動する静電容量も大きくなり、インバータ・バッファ4，5での充放電電流も多くなってしまい、ICの消費電流が多くなってしまうという問題があった。

〔目的〕

本発明はこのような問題点を解決するもので、その目的とするところは、1つの転送クロックで動作するCMOS構造のフリップ・フロップ回路を提供することにある。

〔概要〕

本発明のCMOS構造のフリップ・フロップ回路は、入力データを一方のチャンネルのMOSトランジスタよりなるスイッチ回路でマスタ側データ記憶回路に き込み、マスタ側の記憶データを他方のチャンネルのMOSトランジスタよりなるスイッチ回路でスレーブ側データ記憶回路に転送し、更にマスタ側の転送クロックとスレーブ側の転送クロックに同一の信号を用いることができることを特徴とする。

〔実施例〕

以下、本発明について実施例に基づき詳細に説明する。

第7図は本発明によるフリップ・フロップ回路の基本回路の例であり、マスタ側のデータ記憶回路6の信号Mは、入力データ信号$\overline{DIN}$（入力データ信号DINの逆相信号）が'H'（VDDレベル）で転送クロック信号CL1が'H'のとき、NMOSトランジスタよりなるスイッチ回路8がONして強制的に'L'（VSSレベル）になり、同様にNMOSトランジスタよりなるスイッチ回路7はOFFして信号$\overline{M}$は'H'になる。また入力データ信号DINが'H'の場合は、スイッチ回路7がONして信号$\overline{M}$が強制的に'L'になり、スイッチ回路8はOFFして信号Mは'H'になる。このように入力データDINは、転送クロック信号CL1が'H'のときマスタ側データ記憶回路6へ転送できる。またマスタ側の記憶データをスレーブ側

のデータ記憶回路9に転送するには、信号CL2を'L'にすればよく、マスタ側の信号Mが'H'で信号$\overline{M}$が'L'のとき、スレーブ側のPMOSトランジスタよりなるスイッチ回路11がONして信号Qを強制的に'H'にし、同様にPMOSトランジスタよりなるスイッチ回路10がOFFして信号$\overline{Q}$が'L'になる。またマスタ側の信号Mが'L'で信号$\overline{M}$が'H'のときは、スイッチ回路10がONし、スイッチ回路11がOFFして、信号$\overline{Q}$を強制的に'H'にして信号QがLになる。

このようにマスタ側の記憶データは、転送クロック信号CL2が'L'のときスレーブ側データ記憶回路9へ転送できる。

以上述べたように第7図の回路では、信号CL1が'H'で入力データをマスタ側のデータ記憶回路へ転送し、信号CL2が'L'でマスタ側の記憶データをスレーブ側の記憶回路へ転送することができる。このように信号CL1と信号CL2は'H'と'L'で各々動作するので、同一の信号を用いることができる。

第7図の場合、マスタ側のデータ転送用のスイッチ回路7，8の能力はデータ記憶回路6の論理ゲートの能力より大きくなければならないが、第8図の抵抗18を用いることによりスイッチ回路7，8の能力は第7図のそれに比べて小さくできる。またスレーブ側の場合もマスタ側の場合と同様である。

更に第8図のインバータ・バッファ12はマスタ側のデータ・バッファ用であり、能力を大きくすることで、マスタ側のデータを外部に取り出す際には、信号M，信号$\overline{M}$を直接取り出すより能力的に有利である。

第9図は½分周用のフリップ・フロップ回路の本発明による例であり、第7図の信号DINに信号$\overline{Q}$を、また信号$\overline{DIN}$に信号Qを接続したものである。従来例のクロックド・ゲートを用いたフリップ・フロップ回路では、第4図のように信号DINに信号$\overline{Q}$を接続することで½分周用のフリップ・フロップ回路としていた。

第10図はリセット機能付きのフリップ・フロップ回路の本発明の例であり、マスタ側データ記憶回路6とスレーブ側データ記憶回路9の論理ゲートの一方を、2入力NANDゲート14としてリセット機能をもたせる。リセット信号$\overline{RES}$は通常'H'であり、'L'で信号$\overline{M}$，信号$\overline{Q}$を'H'にし、信号M，信号Qは'L'になり、マスタ側データ記憶回路6，スレーブ側データ記憶回路9がリセットされる。またマスタ側スイッチ回路7に直列接続されるNMOSトランジスタ15は、マスタ側の信号$\overline{M}$が、転送クロック信号CL1が'H'で入力データ信号DINが'H'のとき'L'になることを禁止するためのものであるが、リセット信号$\overline{RES}$が'L'になるタイミングが信号CL1が'L'のときか、または入力データ信号DINが'L'のときか、または入力データ信号DINが'L'のときだけであれば不要である。

第11図はリセット機能付きのフリップ・フロップ回路の本発明による別の例であり、リセット信号$\overline{RES}$を'L'にすることにより、PMOSトランジスタ16をONして、信号$\overline{M}$，信号$\overline{Q}$を強制的に'H'にして、信号M，信号Qを'L'にし、マスタ側データ記憶回路6とスレーブ側データ記憶回路9をリセットする。ここで第11図のNMOSトランジスタは第10図のそれと同じ機能を有するものである。

（効果）

以上述べたように本発明によれば、フリップ・フロップ回路のマスタ側の転送クロックとスレーブ側の転送クロックに同一の信号を用いることができ、従来の2相クロックのものと比べ信号を1つ少なくできるという効果を有し、また2相クロックの場合の位相差t_1，t_2による誤動作もなくなるという効果がある。また信号を1つ少なくすることによりICの面積が小さくなり、ICの単価を安くでき、更に消費電流も少なくできるという効果を有する。その上本発明によれば、フリップ・フロップ回路の素子数を従来のものに比べ少なくできるという効果も有する。第1図の従来の場合、素子数20個であり、第7図の本発明の場合、素子数は16個である。

尚本発明の説明では、マスタ側のスイッチ回路をNMOSトランジスタで構成し、スレーブ側のスイッチ回路をPMOSトランジスタで　成したが、マスタ側のスイッチ回路をPMOSトランジスタ，スレーブ側のスイッチ回路をNMOSトランジスタで構成してもよい。

図面の簡単な説明

第1図はクロックド・ゲートを用いたフリップ・フロップ回路の従来例。

第2図はトランスミッション・ゲートを用いたフリップ・フロップ回路の従来例。

第3図(a)はクロックド・ゲートのシンボル図であり、(b)はクロックド・ゲートの素子構成を示したものである。

第4図はクロックド・ゲートを用いた½分周用のフリップ・フロップ回路の従来例。

第5図は第1図，第2図に用いている信号CLと信号$\overline{CL}$の位相を示したタイミング図。

第6図は複数の従来のフリップ・フロップ回路をシフト・レジスタとして用いたときの接続例である。

第7図は本発明によるフリップ・フロップ回路の基本回路の一例である。

第8図は本発明によるフリップ・フロップ回路の応用の一例である。

第9図は本発明による½分周用のフリップ・フロップ回路の一例である。

第10図，第11図はリセット機能付きの本発明によるフリップ・フロップ回路の一例である。

以　上

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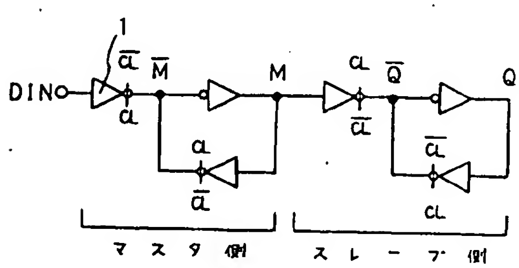
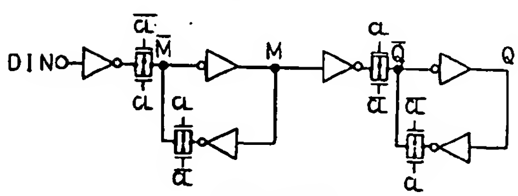
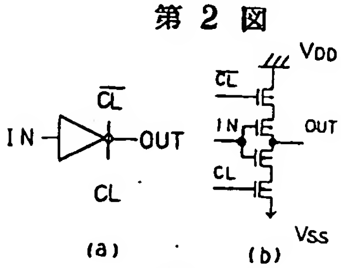
代理人　弁理士　最上　務



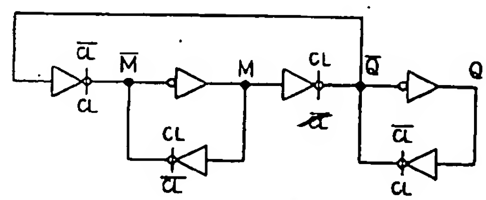
第1図



第2図



第3図



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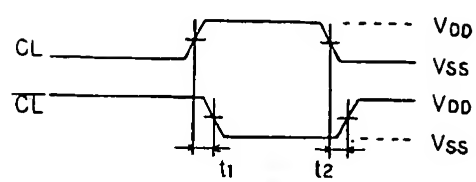
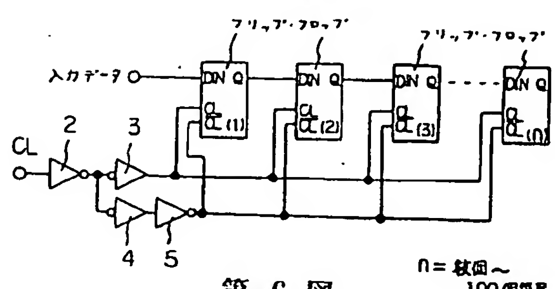
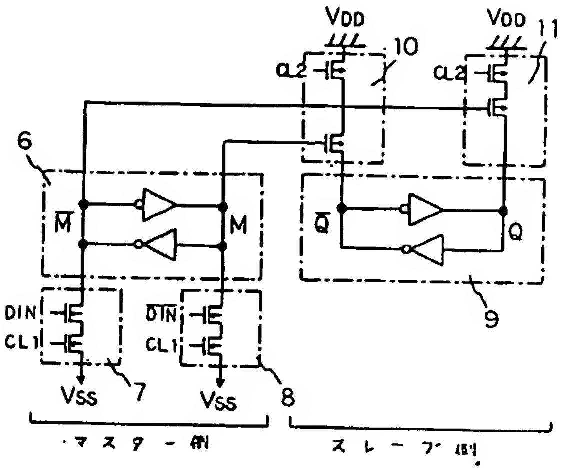


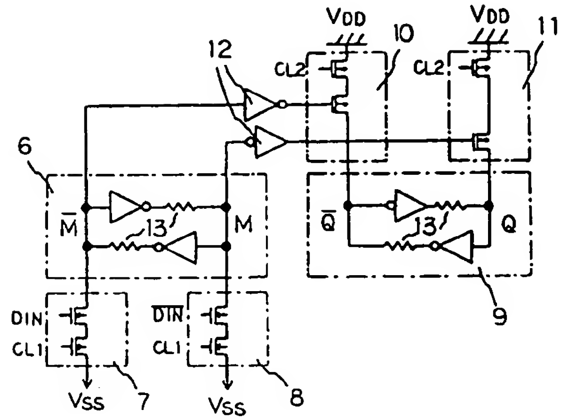
第5図



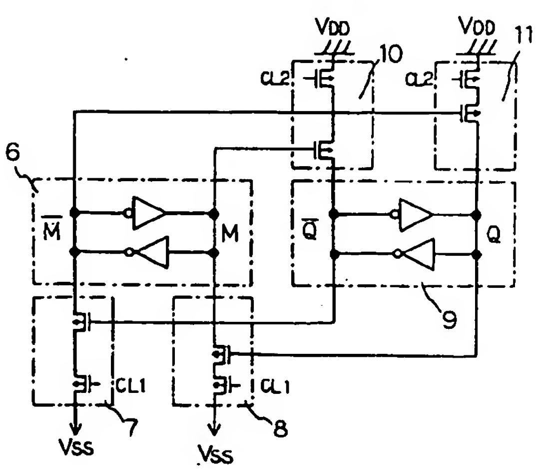
第6図



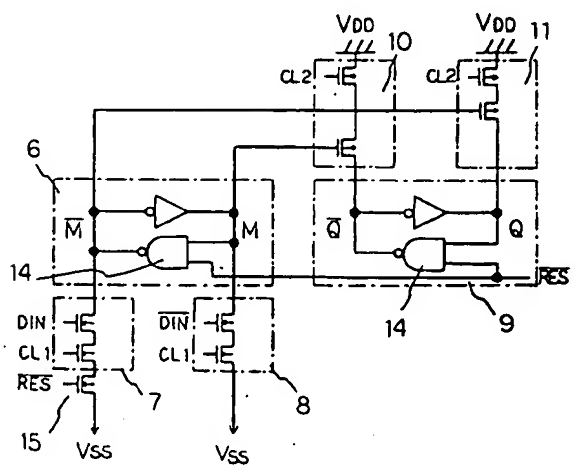
第 7 図



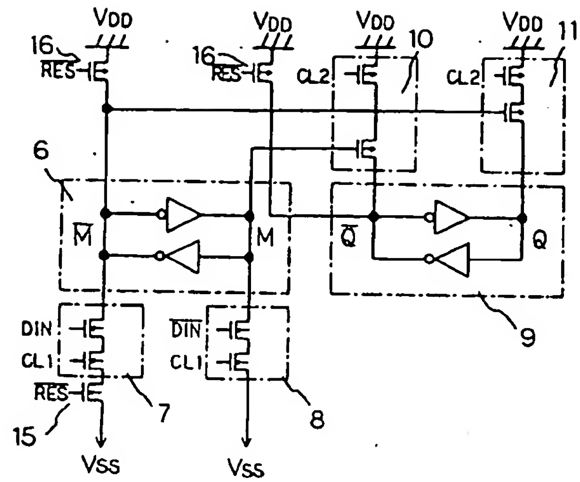
第 8 図



第 9 図



第10図


VDD
VDD
VDD
VDD
16
RES
16
RES
CL2
CL2
10
11
6
M
M
Q
Q
9
DIN
CL1
RES
DIN
CL1
7
8
15
Vss
Vss

第11図

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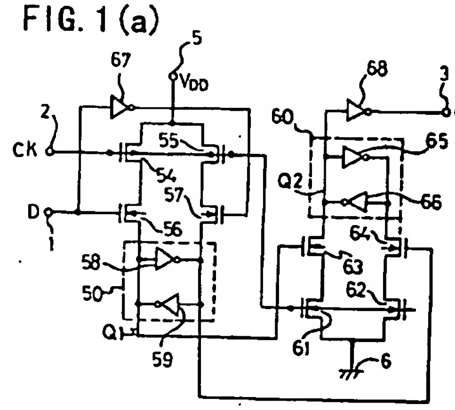
(54) Flip-Flop Circuit

(57) A master-slave type flip-flop circuit includes a master latch circuit and a slave latch circuit. The master latch circuit includes transfer gates (54, 55) for switching between on and off states in response to a clock signal (CK), transfer gates (56, 57) individually connected in series to the transfer gates (54, 55) for switching between on and off states in response to a data signal (D), and a latch section (50) formed from invertors (58, 59) connected to the latter transfer gates (56, 57). The slave latch circuit includes transfer gates (61, 62) for switching between on and off states in response to the clock signal (CK), transfer gates (63, 64) individually connected in series to the transfer gates (61, 62) for switching between on and off states in response to an output and an inverted output of the latch section (50), and a latch section (60) formed from invertors (65, 66) connected to the latter transfer gates (63, 64).

FIG. 1 (a)



EP 0 793 342 A2

Description

This invention relates to a flip-flop circuit, and more particularly to a master-slave type flip-flop circuit.

Several exemplary ones of conventional flip-flop circuits will be described with reference to the accompanying drawings. FIG. 5(a) shows in circuit diagram a construction of an exemplary one of conventional flip-flop circuits. Referring to FIG. 5(a), the flip-flop circuit shown has a data input terminal 1 for receiving a data input signal D, a clock input terminal 2 for receiving a clock input signal CK, and an output terminal 3 for outputting a data output signal Q. The flip-flop circuit includes four transfer gates 88, 89 and 92, 93 and six invertors 90, 91 and 94 to 97 connected between the input and output terminals 1 to 3 such that they form a master-slave type flip-flop circuit. In the flip-flop circuit, the transfer gates 88 and 89 and the invertors 90 and 91 form a master latch circuit, and the transfer gates 92 and 93 and the invertors 94 and 95 form a slave latch circuit.

A timing chart when the master-slave type flip-flop circuit described above operates is shown in FIG. 5(b). Referring to FIG. 5(b), when the clock input signal CK has a low ("L") level, the transfer gate 88 exhibits a conducting state, and an inverted signal to the data input signal D is outputted to an output Q1 of the master latch circuit. Then, when the clock input signal CK changes to a high ("H") level, the transfer gates 89 and 92 are rendered conducting, and the master latch circuit holds data and an inverted signal to the output Q1 is outputted to the output Q of the slave latch circuit.

In the master-slave type flip-flop circuit just described, even if the data input signal D exhibits no change, the outputs of the invertors 96 and 97 change each time the clock input signal CK changes. Consequently, power is consumed by the invertors 96 and 97, and the power consumption increases in proportion to the operation frequency. Further, since the clock input signal CK is inputted to the transfer gates 88, 89 and 92, 93 through the invertors 96 and 97, time is required after a change of the clock input signal till a change of the output signal Q, and this increases the transfer delay time as a flip-flop circuit.

One of countermeasures for overcoming this drawback is disclosed in Japanese Patent Laid-Open Application No. Heisei 1-286609. FIG. 6(a) is a circuit diagram of the circuit shown in the figure 1 of the document just mentioned. Referring to FIG. 6(a), the circuit shown includes a master latch circuit 11 for sampling and latching a data input signal VI when a latch signal VB exhibits the "H" level, a slave latch circuit 12 for sampling and latching an output signal VC of the master latch circuit 11 when the latch signal VB exhibits the "L" level, an invertor 13 for inverting the latch signal VB and supplying the inverted latch signal to the slave latch circuit 12, an EX-OR (exclusive OR) circuit 14 for exclusively ORing an output signal VO of the slave latch circuit 12 and the data input signal VI, and a NAND circuit 15 for logically NANDing an output signal VA of the EX-OR circuit 14 and a clock input signal CK and outputting a latch signal VB.

Since the input signal VI and the output signal VO have an equal level unless the data input signal VI exhibits a change, the output signal VA is fixed to the "L" level and invalidates the clock signal CK to fix the latch signal VB to the "H" level. If the input signal VI changes, then the output signal VA changes to the "H" level, and the NAND circuit 15 validates the clock signal CK so that the master latch circuit 11 and the slave latch circuit 12 individually perform latching operations similarly as in an ordinary flip-flop. Consequently, the output of the entire circuit changes. In this instance, since the input signal VI and the output signal VO exhibit an equal level, unless the input signal VI exhibits a change again, the clock signal CK is invalidated by the EX-OR circuit 14.

A timing chart when the circuit described above operates is shown in FIG. 6(b). Referring to FIG. 6(b), when, in the operation within a period defined by two vertical broken lines in FIG. 6(b), the input signal VI changes from the "L" level to the "H" level while the clock signal CK is at the "H" level, since the level of the output signal VO and the level of the input signal VI are different from each other, the signal VA is changed to the "H" level by the EX-OR circuit 14. In this instance, since the clock input signal CK is at the "H" level, the latch signal VB is changed from the "H" level to the "L" level by the NAND circuit 15, and the master latch circuit 11 latches the signal level at the point of time when the data input signal VI changes to the "H" level since the latch signal VB has been at the "H" level till then, and outputs the latched signal level to the output VC of the master latch circuit 11. Here, since the latch signal VB changes to the "L" level, the "H" level of the output signal VC of the master latch circuit 11 is latched by the slave latch circuit 12, and the thus changing data are outputted as the output signal VO.

In this manner, as seen from the signal waveform VO of FIG. 6(b), depending upon the inputting timings of the input signal VI and the clock signal CK, the flip-flop circuit performs in such an operation as indicated by a broken line different from a normal operation indicated by a solid line, and data are outputted from the flip-flop circuit but not in synchronism with the clock signal CK. Consequently, the flip-flop circuit is disadvantageous in that it malfunctions in this regard.

Further, since the flip-flop circuit requires, in addition to such master latch circuit 11 and slave latch circuit 12 as are required by an ordinary flip-flop circuit, the EX-OR circuit 14 and the NAND circuit 15 for producing the latch signal VB, the flip-flop circuit is advantageous also in that a comparatively large number of elements are required to construct the entire flip-flop.

Furthermore, since the clock input signal CK is inputted to the master latch circuit 11 and the slave latch circuit 12 after it passes the NAND circuit 15 and the invertor 13, time is required after a change of the clock input signal CK till a change of the output signal VO, and

this increases the propagation delay time as a flip-flop circuit.

Another flip-flop circuit which contemplates reduction in power consumption is disclosed in Japanese Patent Laid-Open Application No. Heisei 2-34018. FIG. 7(a) is a circuit diagram shown in the figure 1 of the document just mentioned. Referring to FIG. 7(a), the flip-flop circuit shown includes a pair of transfer gates 31 and 32 which are switched between on and off in response to a clock input signal CK from the outside, a pair of invertors 41 and 42 connected in series in order in a forward direction to the transfer gates 31 and 32, respectively, another pair of transfer gates 33 and 34 connected in cross connection between input and output points of the invertors 41 and 42 and individually switchable between on and off in response to an opposite phase clock input signal $\overline{CK}$ having a phase opposite to that of the clock input signal CK, a further pair of transfer gates 35 and 36 connected to the output points of the invertors 41 and 42, respectively, and individually switchable between on and off in response to the opposite phase clock input signal $\overline{CK}$, another pair of invertors 43 and 44 connected in series in order in a forward direction between the transfer gates 35 and 36 and an output signal Q and an inverted output signal $\overline{Q}$, respectively, and a still further pair of transfer gates 37 and 38 connected in cross connection between input and output points of the invertors 43 and 44 and individually switchable between on and off in response to the clock input signal CK.

In this flip-flop circuit, the transfer gates 31 and 32 are turned on in response to a rising edge of the clock input signal CK from the "L" to the "H" level to fetch a data input signal D and an opposite phase data input signal $\overline{D}$ into a master latch circuit 100.

Then, when the clock input signal CK falls from the "H" to the "L" level, the transfer gates 33 and 36 are turned on, and the master latch circuit 100 holds the data input and simultaneously transfers the data to a slave latch circuit 200. Those data are outputted as the output signal Q and the opposite phase output signal $\overline{Q}$ of the slave latch circuit 200.

FIG. 7(b) shows a timing chart when the flip-flop circuit described above operates. Referring to FIG. 7(b), when, in the operation at a time indicated by a left side one of two vertical broken lines, the clock input signal CK changes from the "L" level to the "H" level, the inverted clock input signal $\overline{CK}$ changes from the "H" level to the "L" level after a fixed delay time. As a result, the transfer gates 31 to 38 are rendered conducting, and the data input signal D and the output signal Q are connected to each other by the transfer gates 31, 34, 36 and 37. Meanwhile, the opposite phase data input signal $\overline{D}$ and the opposite phase output signal $\overline{Q}$ are connected to each other by the transfer gates 32, 33, 35 and 38. Consequently, inputs SL to the slave circuit become unstable, and it is indefinite data of which one of the levels should be latched. In this manner, the flip-flop circuit of FIG. 7(a) sometimes malfunctions such that, when the clock input signal CK changes from the "L" level to the "H" level while the data input signal D and the output signal Q have different levels from each other, as seen from the signal waveform of the output Q of the slave latch circuit, the flip-flop circuit performs such an operation as indicated by a broken line different from a normal operation indicated by a solid line.

Further, since the circuit construction described above requires a clock input signal CK and an inverted clock input signal $\overline{CK}$, naturally an invertor for generation of the inverted clock signal is required. Since this invertor operates irrespective of a change in data, the flip-flop circuit is disadvantageous also in that the power consumption reduction effect is low and the power consumption increases in proportion to the operation frequency.

Further, time is required after a change of the clock input signal CK till a change of the output signal Q, and this increases the propagation delay time as a flip-flop.

In summary, the conventional flip-flop circuits described above are disadvantageous in the following points. First, with the flip-flop circuits shown in FIGS. 5(a) and 7(a), since an invertor for generating an inverted clock signal operates continuously even if the input data D does not change and the output data does not change, the power consumption increases in proportion to the operation frequency. This is because, since two input signals of the clock input signal CK and the inverted clock input signal $\overline{CK}$ are required from the circuit construction, two invertors for generating the inverted clock signal such as the inverters 96 and 97 in the flip-flop circuit of FIG. 5(a) naturally operate continuously irrespective of presence or absence of a change of the input data D.

Second, with the flip-flop circuit shown in FIG. 6(a), an input timing of the clock input signal CK and an input timing of the data input signal VI have a restriction in timing therebetween for stabilization of the circuit. This is because the circuit shown in FIG. 6(a) malfunctions if the level of the data input signal D changes when the clock input signal CK is at the "H" level. Further, the circuit shown in FIG. 7(a) malfunctions at a rising edge of the clock input signal CK when the input data and the output signal Q are different from each other if a delay difference appears between the clock input signal CK and the opposite phase clock input signal $\overline{CK}$.

Third, the flip-flop circuit shown in FIG. 6(a) is composed of a comparatively large number of elements and requires a comparatively large occupation area in a chip. This is because the circuit shown in FIG. 6(a) requires, in addition of the master latch circuit 11 and the slave latch circuit 12, the EX-OR circuit 14, the NAND circuit 15 and the invertor 13 in order to produce the latch signal VB.

Fourth, the circuits shown in FIGS. 5(a) and 6(a) are not suitable for high speed operation because time is required after a change of the clock input signal CK to a change of the data output signal Q or VO. This is because, since the clock input signal CK is inputted to

the transfer gates via the invertors, time is required after a change in level of the clock input signal CK till a change in level of the output signal Q or VO.

It is an object of the present invention to provide a master-slave type flip-flop circuit which is composed of a reduced number of circuit components to reduce power consumption when input data does not exhibit a change to achieve reduction in power consumption and high speed operation.

In order to attain the object described above, according to the present invention, there is provided a master-slave type flip-flop circuit, comprising a master latch circuit for fetching or latching an external data input signal in synchronism with an external clock signal, the master latch circuit including first latch means for complementarily latching data on a first signal line and data on a second signal line, a slave latch circuit connected to the master latch circuit for fetching or latching data signals outputted from the master latch circuit in synchronism with the clock signal, the slave latch circuit including second latch means for complementarily latching data on a third signal line and data on a fourth signal line, the master-slave type flip-flop circuit operating with power supplied from first and second power supply voltage supplying means having different potentials, first current paths provided between the first and second signal lines and the first power supply voltage supplying means and second current paths provided between the third and fourth signal lines and the second power supply voltage supplying means such that the complementary data to be latched by the first latch means are defined by a voltage supply from the first power supply voltage supplying means to the first or second signal line whereas the complementary data to be latched by the second latch means are defined by a voltage supply from the second power supply voltage supplying means to the third or fourth signal line, and a first transfer gate for connecting or disconnecting the first current paths and a second transfer gate for connecting or disconnecting the second current paths, the first and second transfer gates being controlled between conducting and non-conducting states in response to the external clock signal, the external data input signal and the data signals from the first and second signal lines.

In the master-slave type flip-flop circuit, the external clock input signal is inputted directly to the transfer gates without passing a logic gate circuit. Consequently, when the data input signal inputted to the flip-flop circuit does not exhibit a change, no component consumes power irrespective of any change of the clock signal input. Accordingly, the power consumption is reduced as much, and the flip-flop circuit is low in power consumption. Further, since a result when the clock input signal is inputted directly to the transfer gates and the transfer gates are rendered conducting or non-conductive in response to the clock input signal is outputted, for example, through an invertor stage, the delay time after a change of the clock input signal till a change of the output signal at the output terminal is reduced, and consequently, the master-slave type flip-flop circuit is suitable for high speed operation.

Further, since the clock input signal and the data input signal are inputted directly and independently of each other to the transfer gates, such transfer gates as are formed from MOS transistors connected in a complicated connection or a logic gate circuit for generation of a latch signal is not required. Consequently, the master-slave type flip-flop circuit can achieve reduction in number of components, and this can reduce an occupation area of the master-slave type flip-flop circuit on a chip of an integrated circuit. Accordingly, high density integration can be achieved by the master-slave type flip-flop circuit. Further, since the transfer gate to which the data input signal is inputted and the transfer gate to which the clock input signal is inputted operate independently of each other, the clock input signal and the data input signal have no restriction in input timings for stabilization operation.

The above and other objects, features and advantages of the present invention will become apparent from the following description and the appended claims, taken in conjunction with the accompanying drawings in which like parts or elements are denoted by like reference characters.

FIG. 1(a) is a circuit diagram of a flip-flop circuit showing a first preferred embodiment of the present invention;
FIG. 1(b) is a time chart illustrating operation of the flip-flop circuit of FIG. 1(a);
FIG. 2(a) is a circuit diagram of another flip-flop circuit showing a second preferred embodiment of the present invention;
FIG. 2(b) is a time chart illustrating operation of the flip-flop circuit of FIG. 2(a);
FIG. 3 is a circuit diagram of a further flip-flop circuit showing a third preferred embodiment of the present invention;
FIG. 4 is a block diagram of a serial to parallel conversion circuit to which a flip-flop circuit according to the present invention is applied;
FIG. 5(a) is a circuit diagram showing an exemplary one of conventional flip-flop circuits;
FIG. 5(b) is a time chart illustrating operation of the flip-flop circuit of FIG. 5(a);
FIG. 6(a) is a circuit diagram showing another exemplary one of conventional flip-flop circuits;
FIG. 6(b) is a time chart illustrating operation of the flip-flop circuit of FIG. 6(a);
FIG. 7(a) is a circuit diagram showing a further exemplary one of conventional flip-flop circuits; and
FIG. 7(b) is a time chart illustrating operation of the flip-flop circuit of FIG. 7(a).

Referring first to FIG. 1(a), there is shown in circuit diagram a master-slave type flip-flop circuit according to a first preferred embodiment of the present invention.

The master-slave type flip-flop circuit has a clock input terminal 2 for receiving a clock input signal CK, a data input terminal 1 for receiving a data input signal D, and an output terminal 3 for outputting a output signal Q. A terminal of a first PMOS transfer gate 54 is connected to a power supply line 5, and also a terminal of a second PMOS transfer gate 55 is connected to the power supply line 5. The gate electrodes of the first and second PMOS transfer gates 54 and 55 are connected commonly to the clock input terminal 2, and the other terminal of the first PMOS transfer gate 54 is connected to a terminal of a third NMOS transfer gate 56 while the other terminal of the second PMOS transfer gate 55 is connected to a terminal of a fourth NMOS transfer gate 57. The gate electrode of the third NMOS transfer gate 56 is connected to the data input terminal 1, and also an input point of a first invertor 67 is connected to the data input terminal 1. The gate electrode of the fourth NMOS transfer gate 57 is connected to an output point of the first invertor 67, and the other terminal of the third NMOS transfer gate 56 is connected to an input point of a second invertor 58. The other terminal of the fourth NMOS transfer gate 57 is connected to an output point of the second invertor 58, and the output point of the second invertor 58 is connected to an input point of a third invertor 59. An output point of the third invertor 59 is connected to the input point of the second invertor 58. The second and third invertors 58 and 59 form a master latch section 50.

A terminal of a fifth NMOS transfer gate 61 is connected to a ground line 6, and also a terminal of a sixth NMOS transfer gate 62 is connected to the ground line 6. The gate electrodes of the fifth and sixth NMOS transfer gates 61 and 62 are connected commonly to the clock input terminal 2, and the other terminal of the fifth NMOS transfer gate 61 is connected to a terminal of a seventh NMOS transfer gate 63 while the other terminal of the sixth NMOS transfer gate 62 is connected to a terminal of an eighth NMOS transfer gate 64. The gate electrode of the seventh NMOS transfer gate 63 is connected to an output point of the third invertor 59 which forms the master latch section 50, and the gate electrode of the eighth NMOS transfer gate 64 is connected to an output point of the second invertor 58 which constructs the master latch circuit. The other terminal of the seventh NMOS transfer gate 63 is connected to an input point of a fourth invertor 65 and the other terminal of the eighth NMOS transfer gate 64 is connected to an output point of the fourth invertor 65, and the output point of the fourth invertor 65 is connected to an input point of a fifth invertor 66 and an output point of the fifth invertor 66 is connected to an input point of the fourth invertor 65. Thus, the fourth and fifth invertors 65 and 66 form a slave latch section 60. Further, an input point of a sixth invertor 68 is connected to the output point of the fourth invertor 66, and an output point of the sixth invertor 68 is connected to the output terminal 3.

The first and second PMOS transfer gates 54 and 55 are conducting when the clock input signal CK is at the "L" level whereas the fifth and sixth NMOS transfer gates 61 and 62 are conducting when the clock input signal CK is at the "H" level. On the other hand, the third NMOS transfer gate 56 is conducting when the data input signal D is at the "H" level where as the fourth NMOS transfer gate 57 is conducting when the data input signal D is at the "L" level. Further, the seventh and eighth NMOS transfer gates 63 and 64 are switched between conducting and non-conducting states in response to the output of the master latch circuit 50.

FIG. 1(b) is a timing chart when the circuit shown in FIG. 1(a) operates. Referring to FIG. 1(b), when the clock input signal CK changes from the "H" level to the "L" level, the first and second PMOS transfer gates 54 and 55 are rendered conducting. In this instance, since the data input signal D is at the "H" level, the third NMOS transfer gate 56 is rendered conducting, but the fourth NMOS transfer gate 57 is rendered non-conducting because an inverted signal to the data input signal D is inputted thereto from the first invertor 67.

The output Q1 of the master latch section 50 exhibits the "H" level equal to the potential of the power supply line 5 since the first PMOS transfer gate 54 and the third NMOS transfer gate 56 are in a conducting state, and the master latch section 50 holds the data of the "H" level.

When the clock input signal CK changes from the "L" level to the "H" level, the first and second PMOS transfer gates 54 and 55 are rendered non-conducting and simultaneously the fifth and sixth NMOS transfer gates 61 and 62 are rendered conducting. In this instance, since the output Q1 of the master latch section 50 and an inverted signal to the output Q1 are inputted to the seventh and eighth NMOS transfer gates 63 and 64, respectively, and the output signal Q1 of the master latch section 50 is "H" level data, the seventh NMOS transfer gate 63 is rendered conducting while the eighth NMOS transfer gate 64 is rendered non-conducting.

The output signal Q2 of the slave latch section 60 exhibits the "L" level equal to the potential of the ground line 6 since the fifth and seventh NMOS transfer gates 61 and 63 are conducting, and the slave latch section 60 holds the data of the "L" level. Since the signal Q2 of the "L" level is inverted by the sixth invertor 68 of the slave latch circuit, the output terminal Q outputs a signal of the "H" level.

Due to the circuit construction and the operation described above, the master-slave type flip-flop circuit is advantageous in the following points.

(A) Since the first and second PMOS transfer gates 54 and 55 and the fifth and sixth NMOS transfer gates 61 and 62 are rendered conducting or non-conducting directly in response to the clock input signal CK, an inverted clock input signal and an invertor for production of an inverted clock signal are not required. Accordingly, the master-slave type flip-flop circuit is very low in power consumption and high in operation speed.

(B) Since the first and second PMOS transfer gates 54 and 55 to which the clock input signal CK is inputted and the third and fourth NMOS transfer gates 56 and 57 to which the data input signal D is inputted operate independently of each other, the clock input signal CK and the data input signal D have no restriction in timing therebetween, and normally stable operation is anticipated with the master-slave type flip-flop circuit.

(C) The number of elements which form the flip-flop circuit is comparatively small, and the flip-flop circuit is reduced in occupation area in a chip and facilitates high density integration.

Referring now to FIG. 2(a), there is shown in circuit diagram a master-slave type flip-flop circuit according to a second preferred embodiment of the present invention. The master-slave type flip-flop circuit shown has a clock input terminal 2 for receiving a clock input signal CK, a data input terminal 1 for receiving a data input signal D, and an output terminal 3 for outputting an output signal Q. A terminal of a first NMOS transfer gate 69 is connected to a ground line 6, and also a terminal of a second NMOS transfer gate 70 is connected to the ground line 6. The gate electrodes of the first and second NMOS transfer gates 69 and 70 are connected commonly to the clock input terminal 2, and the other terminal of the first NMOS transfer gate 69 is connected to a terminal of a third NMOS transfer gate 71 and the other terminal of the second NMOS transfer gate 70 is connected to a terminal of a fourth NMOS transfer gate 72. The gate electrode of the third NMOS transfer gate 71 is connected to the data input terminal 1 and also an input point of a first invertor 67 is connected to the data input terminal 1, and the gate electrode of the fourth NMOS transfer gate 72 is connected to an output point of the first invertor 67. The other terminal of the third NMOS transfer gate 71 is connected to an input point of a second invertor 58, and the other terminal of the fourth NMOS transfer gate 72 is connected to an output point of the second invertor 58. The output point of the second invertor 58 is connected to an input point of a third invertor 59, and an output point of the third invertor 59 is connected to the input point of the second invertor 58. The second and third invertors 58 and 59 thus form a master latch section 50.

A terminal of a fifth PMOS transfer gate 73 is connected to a power supply line 5, and also a terminal of a sixth PMOS transfer gate 74 is connected to the power supply line 5. The gate electrodes of the fifth and sixth PMOS transfer gates 73 and 74 are connected commonly to the clock input terminal 2, and the other terminal of the fifth PMOS transfer gate 73 is connected to a terminal of a seventh NMOS transfer gate 75 and the other terminal of the sixth PMOS transfer gate 74 is connected to a terminal of an eighth NMOS transfer gate 76. The gate electrode of the seventh NMOS transfer gate 75 is connected to the output point of the third invertor 59 which forms the master latch section 50, and the gate electrode of the eighth NMOS transfer gate 76 is connected to the output point of the second invertor 58 which forms the master latch section 50. The other terminal of the seventh NMOS transfer gate 75 is connected to an input point of a fourth invertor 65, and the other terminal of the eighth NMOS transfer gate 76 is connected to an output point of the fourth invertor 65. The output point of the fourth invertor 65 and the input point of the fifth invertor 66 are connected each other, and the output point of the fifth invertor 66 is connected to the input point fourth invertor 65. Thus, the fourth and fifth invertors 65 and 66 form a slave latch section 60. An input point of a sixth invertor 68 is connected to the output point of the fifth invertor 66, and an output point of the sixth invertor 68 is connected to the output terminal 3.

The first and second NMOS transfer gates 69 and 70 are conducting when the clock input signal CK is at the "H" level, but the fifth and sixth PMOS transfer gates 73 and 74 are conducting when the clock input signal CK is at the "L" level. Further, the seventh and eighth NMOS transfer gates 75 and 76 are switched between conducting and non-conducting states in response to an output of the master latch section 50.

FIG. 2(b) is a timing chart when the circuit of FIG. 2(a) operates. Referring to FIG. 2(b), when the clock input signal CK changes from the "L" level to the "H" level, the first and second NMOS transfer gates 69 and 70 are rendered conducting. If the data input signal D rises from the "L" level to the "H" level in this condition, then the third NMOS transfer gate 71 is rendered conducting. On the other hand, the fourth NMOS transfer gate 72 is rendered non-conducting because an inverted signal to the data input signal D is inputted thereto from the first invertor 67. As a result, the output Q1 of the master latch section 50 exhibits the "L" level equal to the potential of the ground line 6 since the first and third NMOS transfer gates 69 and 71 are conducting, and the master latch section 50 holds the data of the "L" level.

If the clock input signal CK falls from the "H" level to the "L" level, then the first and second NMOS transfer gates 69 and 70 are rendered non-conducting while the fifth and sixth PMOS transfer gates 73 and 74 are rendered conducting. Since the output Q1 of the master latch section 50 and an inverted signal to the output Q1 are inputted to the seventh and eighth NMOS transfer gates 75 and 76, respectively, and the output Q1 of the master latch section 50 is data of the "L" level, the seventh NMOS transfer gate 75 is rendered non-conducting while the eighth NMOS transfer gate 76 is rendered conducting. As a result, the signal Q2B of the slave latch section 60 exhibits the "H" level equal to the potential of the power supply since the sixth PMOS transfer gate 74 and the eighth NMOS transfer gate 76 ar conducting. Accordingly, the slave latch section 60 holds the data of the "L" level inverted from the signal Q2B. Since the data Q2 of the "L" level is inverted by the sixth invertor 68 connected to the output signal Q2 of the

slave latch section 60, the output terminal 3 outputs a signal Q of the "H" level.

Referring now to FIG. 3(a), there is shown in circuit diagram a master-slave type flip-flop circuit according to a third preferred embodiment of the present invention. The master-slave type flip-flop circuit shown has a clock input terminal 2 for receiving a clock input signal CK, a data input terminal 1 for receiving a data input signal D, and an output terminal 3 for outputting a data output signal Q. A terminal of a first NMOS transfer gate 79 is connected to a power supply line 5, and also a terminal of a second NMOS transfer gate 80 is connected to the power supply line 5. The other terminal of the first NMOS transfer gate 79 is connected to a terminal of a third PMOS transfer gate 77, and the other terminal of the second NMOS transfer gate 80 is connected to a fourth PMOS transfer gate 78. The gate electrode of the second NMOS transfer gate 80 is connected to the data input terminal 1, and also an input point of a first invertor 67 is connected to the data input terminal 1. The gate electrode of the first NMOS transfer gate 79 is connected to an output point of the first invertor 67, and the gate electrodes of the third and fourth PMOS transfer gates 77 and 78 are connected commonly to the clock input terminal 2. The other terminal of the third PMOS transfer gate 77 is connected to an input point of a second invertor 58, and the other terminal of the fourth PMOS transfer gate 78 is connected to an output point of the second invertor 58. The output point of the second invertor 58 is connected to an input point of a third invertor 59, and an output point of the third invertor 59 is connected to the input point of the second invertor 58. The second and third invertors 58 and 59 thus form a master latch section 50.

A terminal of a fifth NMOS transfer gate 83 is connected to a ground line 6, and also a terminal of a sixth NMOS transfer gate 84 is connected to the ground line 6. The gate electrode of the fifth NMOS transfer gate 83 is connected to the output point of the third invertor 59 which forms the master latch section 50, and the gate electrode of the sixth NMOS transfer gate 84 is connected to the output point of the second invertor 58 which forms the master latch section 50. The other terminal of the fifth NMOS transfer gate 83 is connected to a terminal of a seventh NMOS transfer gate 81, and the other terminal of the sixth NMOS transfer gate 84 is connected to a terminal of an eighth NMOS transfer gate 82. The gate electrodes of the seventh and eighth NMOS transfer gates 81 and 82 are connected commonly to the clock input terminal 2. The other terminal of the seventh NMOS transfer gate 81 is connected to an input point of a fourth invertor 65, and the other terminal of the eighth NMOS transfer gate 82 is connected to an output point of the fourth invertor 65. The output point of the fourth invertor 65 is connected to an input point of a fifth invertor 66, and an output point of the fifth invertor 66 is connected to the input point of the fourth invertor 65. The fourth and fifth invertors 65 and 66 thus form a slave latch section 60. An input point of a sixth invertor 68 is connected to the output point of the fifth invertor 66, and an output point of the sixth invertor 68 is connected to the output terminal 3.

The master-slave type flip-flop circuit of FIG. 3 operates basically similar to that of the master-slave type flip-flop circuit of FIG. 1(a). However, since the third and fourth PMOS transfer gates 77 and 78 and the seventh and eighth NMOS transfer gates 81 and 82 which are switched between conducting and non-conducting states in response to a change of the clock input signal CK are connected to positions near to the master latch section 50 or the output terminal 3, the times after a change of the clock input signal CK till a change of the held data by the master latch section 50 and a change of the data output signal Q are short. Consequently, the present master-slave type flip-flop circuit exhibits an improved operation speed.

FIG. 4 shows in circuit diagram an exemplary application of a master-slave type flip-flop circuit according to the present invention. The master-slave type flip-flop circuit of the present invention does not include an element which operates in response to a change of the clock input signal CK and consumes power when the data input signal D does not change as described hereinabove. Consequently, where such master-slave type flip-flop circuits are connected in series as seen in FIG. 4 to construct a series to parallel conversion circuit, the power consumption reduction effect appears significantly, and where a large number of flip-flop circuits are connected in series, the effect is very significant.

Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the spirit and scope of the invention as set forth herein.

Claims

1. A master-slave type flip-flop circuit which includes a master latch circuit for fetching or latching an external data input signal (D) in synchronism with an external clock signal (CK), said master latch circuit including first latch means (50) for complementarily latching data on a first signal line and data on a second signal line, and a slave latch circuit connected to said master latch circuit for fetching or latching data signals outputted from said master latch circuit in synchronism with the clock signal (CK), said slave latch circuit including second latch means (60) for complementarily latching data on a third signal line and data on a fourth signal line, and operates with power supplied from first and second power supply voltage supplying means (5, 6) having different potentials, characterized in that it comprises:

   first current paths provided between said first and second signal lines and said first power supply voltage supplying means (5) and sec-

ond current paths provided between said third and fourth signal lines and said second power supply voltage supplying means (6) such that the complementary data to be latched by said first latch means (50) are defined by a voltage supply from said first power supply voltage supplying means (5) to said first or second signal line whereas the complementary data to be latched by said second latch means (60) are defined by a voltage supply from said second power supply voltage supplying means (6) to said third or fourth signal line; and

a first transfer gate (54 to 57; 69 to 72; 77 to 80) for connecting or disconnecting said first current paths and a second transfer gate (61 to 64; 73 to 76; 81 to 84) for connecting or disconnecting said second current paths, said first and second transfer gates (54 to 57, 61 to 64; 69 to 72, 73 to 76; 77 to 80, 81 to 84) being controlled between conducting and non-conducting states in response to the external clock signal (CK), the external data input signal (D) and the data signals from said first and second signal lines.

2. A master-slave type flip-flop circuit which includes a master latch circuit including first latch means (50) provided between a first signal line and a second signal line for complementarily latching data on said first and second signal lines, and a slave latch circuit including second latch means (60) provided between a third signal line and a fourth signal line for complementarily latching data signals on said third and fourth signal lines, said master latch circuit and said slave latch circuit being connected in cascade connection, and operates with power supplied from first and second power supply voltage supplying means (5, 6) having different potentials, characterized in that

said master latch circuit further includes a transfer gate (54, 55; 69, 70; 77, 78) which is rendered conducting or non-conducting in response to an external clock signal (CK) and another transfer gate (56, 57; 71, 72; 79, 80) which is rendered conducting or non-conducting in response to an external data input signal (D) or an inverted signal to the external data input signal (D) such that said first and second signal lines are alternately connected to said first power supply voltage supplying means (5) in response to the data input signal (D) in synchronism with the clock signal (CK) so that the complementary data of said first and second signal lines are compelled to states defined by the data input signal (D) by the supply voltage from said first power supply voltage supplying means (5), and

said slave latch circuit further includes a transfer gate (61, 62; 73, 74; 81, 82) which is rendered conducting or non-conducting in response to the clock signal (CK) and another transfer gate (63, 64; 75, 76; 83, 84) which is rendered conducting or non-conducting in response to the complementary data from the first and second signal lines of said master latch circuit such that said third and fourth signal lines are alternately connected to said second power supply voltage supplying means (6) in response to the complementary from said first and second signal lines of said master latch circuit in synchronism with the clock signal (CK) so that the complementary data of said third and fourth signal lines are compelled to states defined by the complementary data of said first and second signal lines by the supply voltage from said second power supply voltage supplying means (6).

3. A master-slave type flip-flop circuit which includes a data input terminal (1), a clock input terminal (2), an output terminal (3) and first and second power supplying means (5, 6) for supplying different voltages, characterized in that it comprises:

a master latch circuit including first and second transfer gates (54, 55; 69, 70; 77, 78) which are rendered conducting or non-conducting in response to a clock signal (CK), third and fourth transfer gates (56, 57; 71, 72; 79, 80) which are rendered conducting or non-conducting in response to a data input signal (D), said first and second transfer gates (54, 55; 69, 70; 77, 78) and said third and fourth transfer gates (56, 57; 71, 72; 79, 80) being connected in series to form first and second signal lines, respectively, and latch means (50) connected at a terminal thereof to said first signal line and at another terminal thereof to said second signal line such that said first and second signal lines are complementary to each other; and

a slave latch circuit including fifth and sixth transfer gages (61, 62; 73, 74; 81, 82) which are rendered conducting or non-conducting in response to the clock signal (CK), seventh and eighth transfer gates (63, 64; 75, 76; 83, 84) which are rendered conducting or non-conducting in response to an output signal of said master latch circuit, said fifth and sixth transfer gates (61, 62; 73, 74; 81, 82) and said seventh and eighth transfer gates (63, 64; 75, 76; 83, 84) being connected in series to form third and fourth signal lines, respectively, and latch means (60) connected at a terminal thereof to said third signal line and at another terminal thereof to said fourth signal line such that said third and fourth signal lines are complementary to each other.

4. A master-slave type flip-flop circuit as set forth in claim 3, characterized in that said first to eighth transfer gates (54 to 57, 63 to 66; 69 to 72, 73 to 76; 77 to 80, 81 to 84) are each formed from a conducting type MOS field effect transistor.

5. A master-slave type flip-flop circuit, characterized in that it comprises:

a master latch circuit including first latch means (50) including a pair of invertors (58, 59) each connected at an input point to an output point of the other invertor for complementarily latching data of first and second signal lines connected to two junction points of said invertors (58, 59), a first p-channel MOS field effect transistor (54) and a second n-channel MOS field effect transistor (56) connected in series in order between a high potential power supply voltage supplying line (5) and said first signal line, and a third p-channel MOS field effect transistor (55) and a fourth n-channel MOS field effect transistor (57) connected in series in order between said high potential power supply voltage supplying line (5) and said second signal line, an external clock signal (CK) being inputted to the gate electrodes of said first and third MOS field effect transistors (54, 55), an external data signal (D) being inputted to the gate electrode of said second MOS field effect transistor (56), an inverted signal to the data signal (D) being inputted to the gate electrode of said fourth MOS field effect transistor (57); and
a slave latch circuit including second latch means (60) including a pair of invertors (65, 66) each connected at an input point to an output point of the other invertor for complementarily latching data of third and fourth signal lines connected to two junction points of said invertors (65, 66), a fifth n-channel MOS field effect transistor (61) and a sixth n-channel MOS field effect transistor (63) connected in series in order between a low potential power supply voltage supplying line (6) and said third signal line, and a seventh n-channel MOS field effect transistor (62) and an eighth n-channel MOS field effect transistor (64) connected in series in order between said low potential power supply voltage supplying line (6) and said fourth signal line, the clock signal (CK) being inputted to the gate electrodes of said fifth and seventh MOS field effect transistors (61, 62), a signal from said first signal line in said master latch circuit being inputted to the gate electrode of said sixth MOS field effect transistor (63), a signal from said second signal line in said master latch circuit being inputted to the gate electrode of said eighth MOS field effect transistor (64).

6. A master-slave type flip-flop circuit, characterized in that it comprises:

a master latch circuit including first latch means (50) including a pair of invertors (58, 59) each connected at an input point to an output point of the other invertor for complementarily latching data of first and second signal lines connected to two junction points of said invertors (58, 59), a first n-channel MOS field effect transistor (69) and a second n-channel MOS field effect transistor (71) connected in series in order between a low potential power supply voltage supplying line (6) and said first signal line, and a third n-channel MOS field effect transistor (70) and a fourth n-channel MOS field effect transistor (72) connected in series in order between said low potential power supply voltage supplying line (6) and said second signal line, an external clock signal (CK) being inputted to the gate electrodes of said first and third MOS field effect transistors (69, 70), an external data signal (D) being inputted to the gate electrode of said second MOS field effect transistor (71), an inverted signal to the data signal (D) being inputted to the gate electrode of said fourth MOS field effect transistor (72); and
a slave latch circuit including second latch means (60) including a pair of invertors (65, 66) each connected at an input point to an output point of the other invertor for complementarily latching data of third and fourth signal lines connected to two junction points of said invertors (65, 66), a fifth p-channel MOS field effect transistor (73) and a sixth n-channel MOS field effect transistor (75) connected in series in order between a high potential power supply voltage supplying line (5) and said third signal line, and a seventh p-channel MOS field effect transistor (74) and an eighth n-channel MOS field effect transistor (76) connected in series in order between said high potential power supply voltage supplying line (5) and said fourth signal line, the clock signal (CK) being inputted to the gate electrodes of said fifth and seventh MOS field effect transistors (73, 74), a signal from said first signal line in said master latch circuit being inputted to the gate electrode of said sixth MOS field effect transistor (75), a signal from said second signal line in said master latch circuit being inputted to the gate electrode of said eighth MOS field effect transistor (76).

7. A master-slave type flip-flop circuit, characterized in that it comprises:

a master latch circuit including first latch means (50) including a pair of invertors (58, 59) each connected at an input point to an output point of

the other invertor for complementarily latching data of first and second signal lines connected to two junction points of said invertors (58, 59), a first n-channel MOS field effect transistor (79) and a second p-channel MOS field effect transistor (77) connected in series in order between a high potential power supply voltage supplying line (5) and said first signal line, and a third n-channel MOS field effect transistor (80) and a fourth p-channel MOS field effect transistor (78) connected in series in order between said high potential power supply voltage supplying line (5) and said second signal line, an inverted signal to an external data signal (D) being inputted to the gate electrode of said first MOS field effect transistor (79), the data signal (D) being inputted to the gate electrode of said third MOS field effect transistor (80), an external clock signal (CK) being inputted to the gate electrodes of said second and fourth MOS field effect transistors (77, 78); and

a slave latch circuit including second latch means (60) including a pair of invertors (65, 66) each connected at an input point to an output point of the other invertor for complementarily latching data of third and fourth signal lines connected to two junction points of said invertors (65, 66), a fifth n-channel MOS field effect transistor (83) and a sixth n-channel MOS field effect transistor (81) connected in series in order between a low potential power supply voltage supplying line (6) and said third signal line, and a seventh n-channel MOS field effect transistor (84) and an eighth n-channel MOS field effect transistor (82) connected in series in order between said low potential power supply voltage supplying line (6) and said fourth signal line, a signal from said first signal line in said master latch circuit being inputted to the gate electrode of said fifth MOS field effect transistor (83), a signal from said second signal line in said master latch circuit being inputted to the gate electrode of said seventh MOS field effect transistor (84), the clock signal (CK) being inputted to the gate electrodes of said sixth and eighth MOS field effect transistors (81, 82).

FIG. 1 (a)

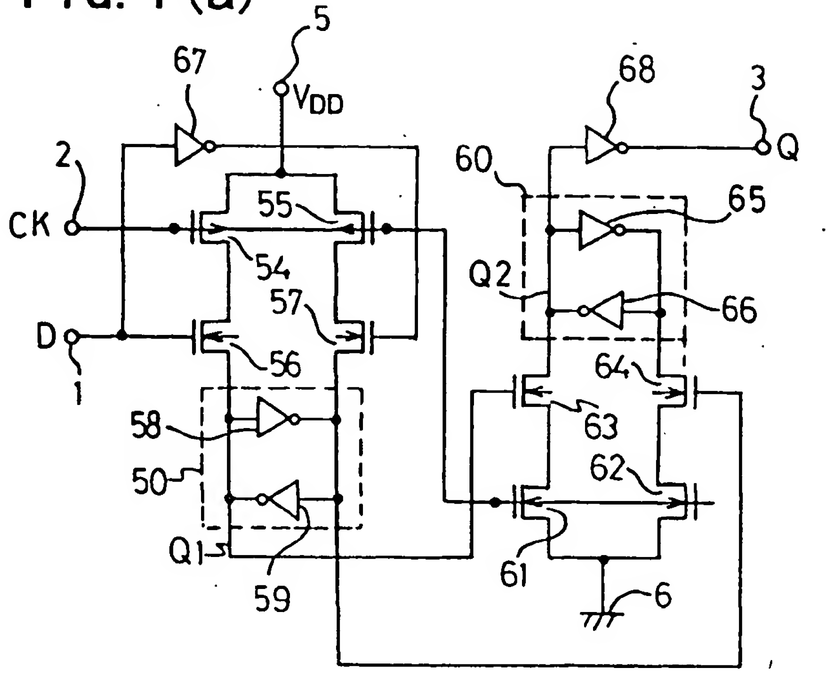

5
67
VDD
68
3
2
Q
60
CK
55
65
54
Q2
57
66
D
56
1
64
58
63
50
62
Q1
61
59
6

FIG. 1 (b)

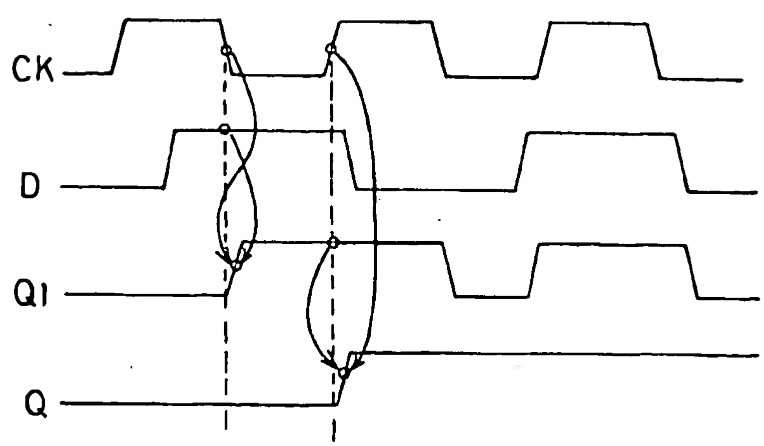

CK
D
Q1
Q

FIG. 2(a)

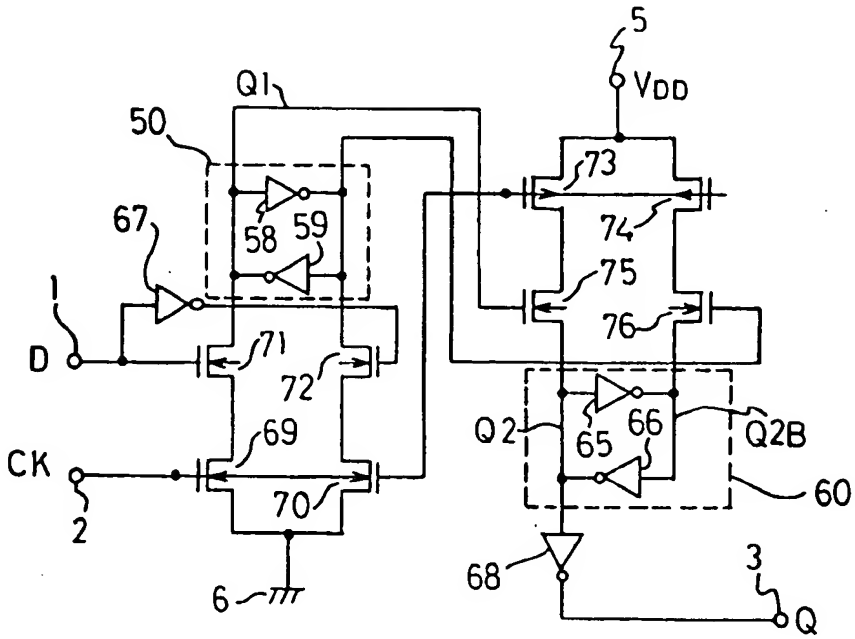

5
VDD
Q1
50
73
74
58
59
67
75
1
76
71
D
72
Q2
66
Q2B
69
65
CK
60
70
2
68
3
6
Q

FIG. 2(b)

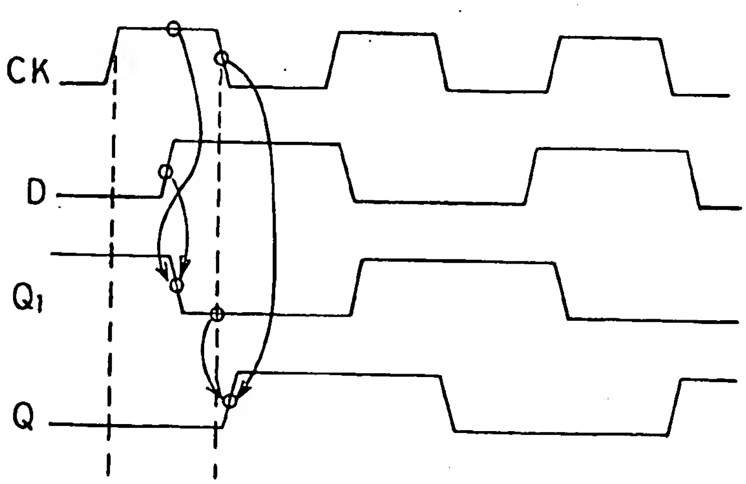

CK
D
Q_1
Q

FIG. 6 (a)

PRIOR ART

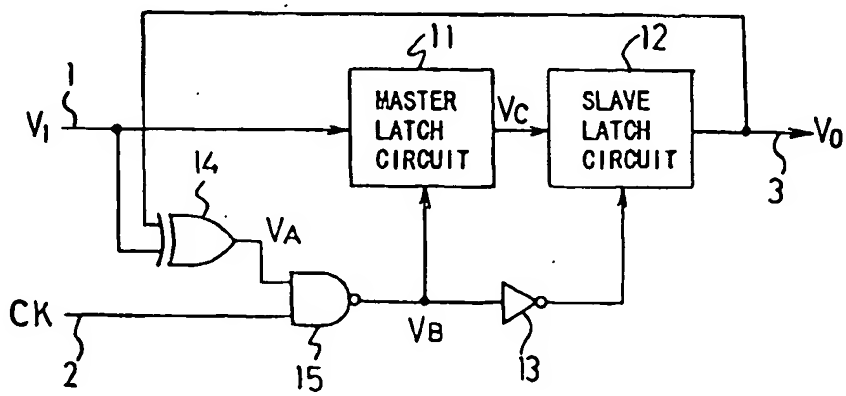


FIG. 6 (b)

PRIOR ART

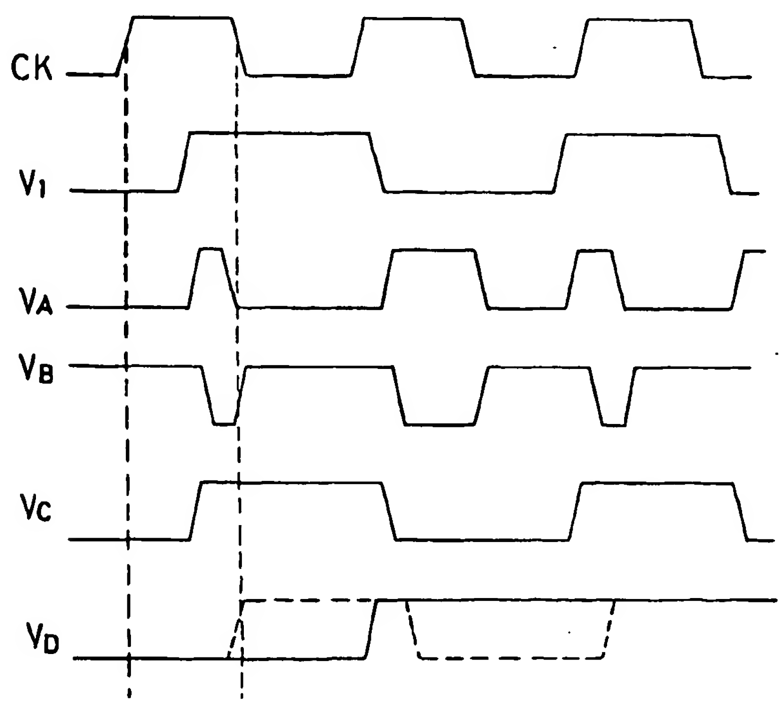


FIG. 7(a)

PRIOR ART

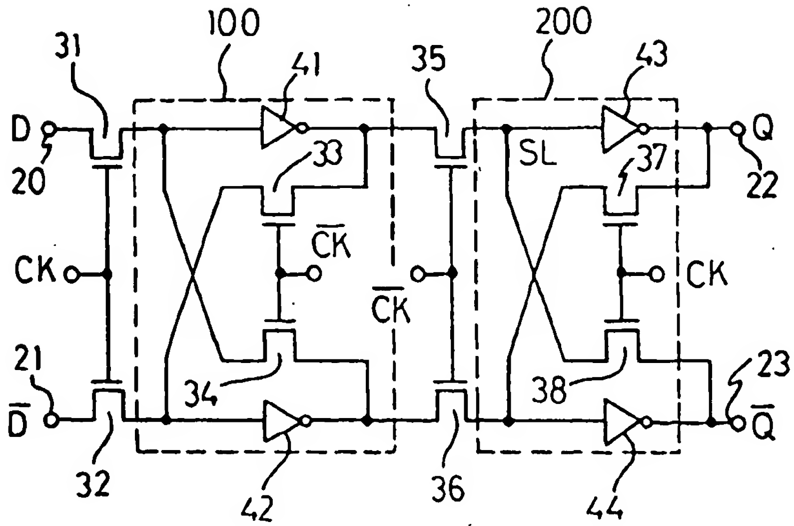


FIG. 7(b)

PRIOR ART